A Leakage power reduction in MOSFET as a Switched-Capacitor Circuits on deep submicron Technology

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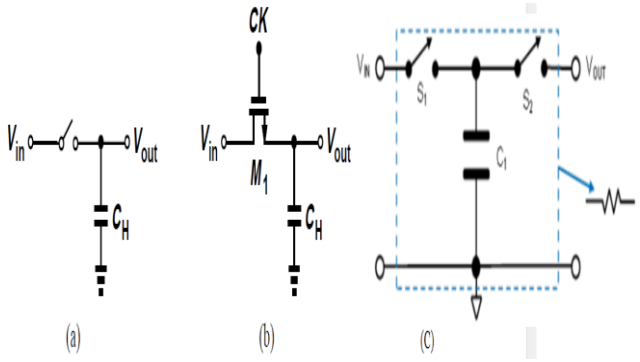
Abstract- Analog, switched-capacitor circuits implement a large class of functions, such as sampling, filtering, and digitization. Moreover, their performance makes them fit for integration with complex, digital-signal-processing blocks in a compatible, low-cost technology mainly in CMOS design. This discussion focuses specifically on CMOS switched-capacitor circuits. The switch capacitor MOSFET is use as a resistor in integrated chip. This switch capacitor circuit exhibits the channel charge injection and clock feed through problems which raise the leakage power dissipation. In this paper a switch capacitor circuit (base on Op-Amp) is discuss which will alleviate these problems of channel charge injection and clock feed through. With these design methods building blocks essential for switched-capacitor circuits can be implemented on deep submicron CMOS design technology. The leakage currents of switch-enabled circuits are characterized across process variations and dissimilar operation voltages in all demonstrated application.

Keywords- SC circuit, charges Injection, Clock feed through, MOSFET.

I. INTRODUCTION

As device dimensions shrink, the applied voltages will require to be proportionately scaled in order to guarantee long-term reliability and control power density. The decrease in supply voltage introduces numerous factors that complicate the design of low-voltage, analog circuits. The characteristic of power optimization makes switched-capacitor (SC) circuits more utilizable building blocks for analog signal processing in battery powered or self-sustained micro power systems. There are many reasons for which power losses arise in CMOS circuit. The different types of leakage components are: Sub-threshold leakage (weak inversion current), Gate oxide leakage (Tunneling current), and Channel punch through, Drain induced barrier lowering. The switch capacitor MOSFET is use as a resistor in integrated chip. This switch capacitor circuit exhibits the channel charge injection and clock feed through problems which increases the leakage power dissipation. In this work a switch capacitor circuit (Op-Amp) is design which will mitigate these problems of channel charge injection and clock feed through.



CMOS Switching circuits (a) Simple sampling circuit, (b) implementation of the switch by a MOS device, (c) Charge In-Out through switch by a MOS device.

Ea Each switching cycle transform a charge q from the input to the output at the switching frequency F. Recall that the charge q on a capacitor with a voltage V between needs is given by:

$$Q = C\,V \quad \ldots\ldots (1)$$

Where V is the voltage across the capacitor.

When switch S1 is close and S2 is open the charge transferred to C to output as

$$Q_{in} = C\,V_{IN} \quad \ldots\ldots (2)$$

When switch S2 is close and S1 is open the charge transferred from C to output as

$$Q_{out} = C\,V_{out} \quad \ldots\ldots (3)$$

The charge change transferred in each cycle is:

$$\Delta q = Q_{out} - Q_{in} = C\,(V_{out} - V_{IN}) \quad \ldots\ldots (4)$$

Since charge q is transferred at rate F, the rate of transfer of charge per unit time is:

$$I = \Delta q\,F \quad \ldots\ldots (5)$$

Thus

$$I = C\,(Vout - V_{IN})\,F$$

$$\text{I.e. } I = C.\Delta V\,F \quad \ldots\ldots (6)$$

Now the relationship between current and voltage shows

$$R = V/I \quad \ldots\ldots (7)$$

Thus

R = 1 / (CF)

Hence the circuit behaves like a resistor whose value depends on C and F. The MOSFET base switch capacitor is always use as a replacement for resistor in integrated chips.

II. Related Work

With the scaling of supply voltage, the voltage accessible to represent the signal is reduced, thus dynamic range becomes a main problem. In order to keep the similar dynamic range on a lower supply voltage, the thermal noise in the circuit must furthermore be proportionately reduced. There, though, exists a trade-off between noise and power consumption. Because of this, it will be shown that in definite conditions, the power consumption will raise as the supply voltage is decreased. In [1] the low leakage power switch capacitor circuit using 0.35um technology is design on body guarded (BG) switch which yields extremely efficient leakage reduction with less additional on-chip components. Simulation results at room temperature, the average absolute leakage current of BG-switch-enabled S/H amplifier, SC amplifier, and DEMOS show leakage current improvement compared with equivalent circuits utilizing transmission gates (TGs). In [2] a logic gates based on the resistive switching random access memory (RRAM) is design. It designs the 1-bit adder and simulates with a prediction of energy consumption. In [3] a power optimized switched-capacitor circuits is design with a lower supply voltage. In order to maintain the same dynamic range on a lower supply voltage requires a quadratic increase in sampling capacitance to reduce thermal noise. The required increase in bias current to maintain circuit bandwidth results in a net increase in the overall power consumption. In [4], a low power switch capacitor is design using NMOS circuits. The size of the NMOS base capacitor was 18 x 18 um, which corresponds to 0.5 pF. C_i consisted of the parallel connection of 10 unit capacitors, while other capacitors are taken as single-unit capacitors. The deglitching capacitor Cdg was connected between the input and output terminals to reduce the generation of output spikes during the non-overlapping period of clock phases.

III. Precision Considerations

Our foregoing study of MOS switches indicates that a larger W=L or a smaller sampling capacitor results in a higher speed. In this section, we show that these methods of increasing the speed degrade the precision with which the signal is sampled. Three mechanisms in MOS transistor operation introduce error at the instant the switch turns off.

IV. Channel Charge Injection

In the "off" state, the gate is grounded and the device is cut off. In the "on" state, a constant voltage of V_{dd} is applied across the gate to source terminals, and a low on-resistance is established from drain to source independent of the input signal. Consider the sampling circuit of Fig. 2 and recall that for a MOSFET to be on, a channel must exist at the oxide-silicon interface. Assuming V_{IN} -V_{out}, then the total charge in the inversion layer as

$$Q_{ch} = AL\ C_{ox}\ (V_{dd} - V_{IN} - V_{th}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (8)$$

Where L denotes the effective channel length. When the switch turns off, Qch exits through the source and drain terminals, a phenomenon called "channel charge injection."

The charge injected to the left side on Fig. is absorbed by the input source, creating no error. On the other hand, the charge injected to the right side is deposited on CH, introducing an error in the voltage stored on the capacitor. For example, if half of Qch is injected onto CH, the resulting error equals

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{TH})}{2C_H} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (9)$$

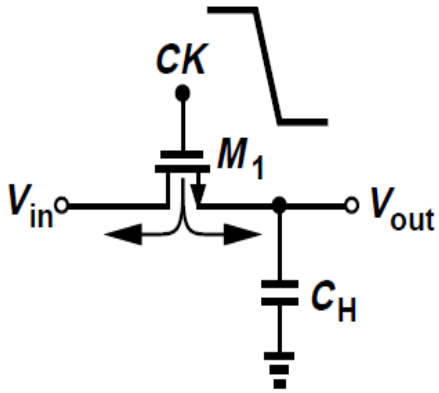


Fig 2: Charge injection when a switch turns off.

Fig 3 below shows the error for an NMOS switch appears as a negative "pedestal" at the output.

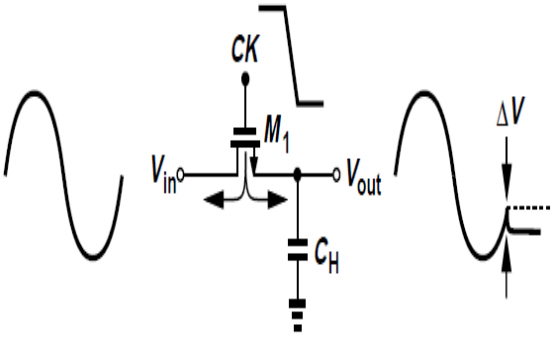


Fig 3: Effect of charge injection.

Note that the error is directly proportional to WLC_{ox} and inversely proportional to CH. An important question that arises now is: why did we assume in arriving at that exactly half of the channel charge in injected onto CH? In reality, the fraction of charge that exits through the source and drain terminals is a relatively complex function of various parameters such as the impedance seen at each terminal to ground and the transition time of the clock. Investigations of this effect have not yielded any rule of thumb that can predict the charge splitting in terms of

such parameters. Furthermore, in many cases, these parameters, e.g., the clock transition time, are poorly controlled. Also, most circuit simulation programs model charge injection quite inaccurately. As a worst-case estimate, we can assume that the entire channel charge is injected onto the sampling capacitor.

How does charge injection affect the precision? Assuming all of the charge is deposited on the capacitor, we express the sampled output voltage as

$$V_{out} \approx V_{in} = \frac{WLC_{ox}(V_{DD}-V_{in}-V_{TH})}{C_H} \quad \ldots\ldots\ldots (10)$$

where the phase shift between the input and output is neglected. Thus,

$$V_{out} = V_{in}\left(1+\frac{WLC_{ox}}{C_H}\right) - \frac{WLC_{ox}(V_{DD}-V_{TH})}{C_H} \ldots.. (11)$$

suggesting that the output deviates from the ideal value through two effects: a non-unity gain equal to1 + WLC_{ox}/C_H a constant offset voltage $-WLC_{ox}$ (V_{DD} - V_{TH}) C_H. In other words, since we have assumed channel charge is a linear function of the input voltage, the circuit exhibits only gain error and dc offset.

Clock Feed through:

In addition to channel charge injection, a MOS switch couples the clock transitions to the sampling capacitor through its gate-drain or gate-source overlap capacitance. Depicted in fig below , the effect introduces an error in the sampled output voltage. Assuming the overlap capacitance is constant, we express the error as

$$\Delta V = V_{CK}\frac{WC_{ov}}{WC_{ov}+C_H} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

where C_{ov} is the overlap capacitance per unit width. The error DV is independent of the input level, manifesting itself as a constant offset in the input/output characteristic. As with charge injection, clock feed through leads to a trade-off between speed and precision as well.

Charge Injection Cancellation:

To arrive at the first technique, we postulate that the charge injected by the main transistor can be removed by means of a second transistor. As shown in Fig. , a "dummy" switch, M2, driven by CK is added to the circuit such that after M1 turns off and M2 turns on, the channel charge deposited by the former on CH is absorbed by the latter to create a channel. Note that both the source and drain of M2 are connected to the output node.

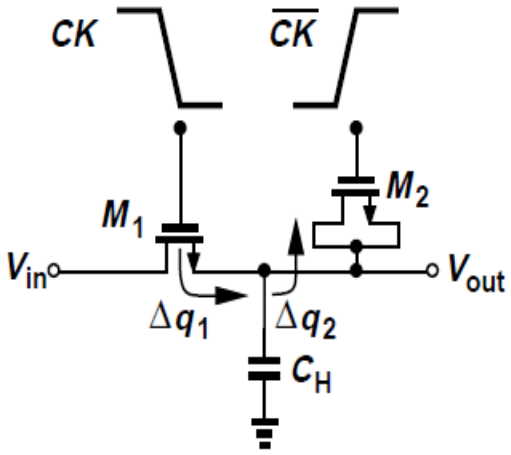


Fig 4: Addition of dummy device to reduce charge injection and clock feed through.

How do we ensure that the charge injected by M1, Dq1, is equal to that absorbed by M2, Dq2? Suppose half of the channel charge of M1 is injected onto CH, i.e.

$$\Delta_{q1} = \frac{WLC_{ox}}{2}(V_{CK} - V_{IN} - V_{TH1}) \ldots\ldots\ldots\ldots\ldots (13)$$

Since $\Delta q_2 = W_2L_2C_{ox}(V_{CK} - V_{IN} - V_{TH2})$, if we choose W2 = $0.5W_1$ and $L_2 = L_1$, then $\Delta q_2 = \Delta q_1$. Unfortunately, the assumption of equal splitting of charge between source and drain is generally invalid, making this approach less attractive.

Interestingly, with the choice W2 = 0:5W1 and L2 = L1, the effect of clock feed through is suppressed. As depicted in Fig. below, the total charge in V_{out} is zero

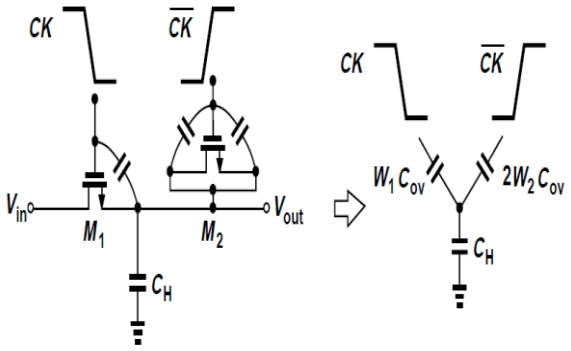


Fig 5: Clock feed through suppression by dummy switch.

$$-V_{CK}\frac{W_1C_{ov}}{W_1C_{ov}+C_{ov}+2W_2C_{ov}} + V_{CK}\frac{2W_2C_{ov}}{W_1C_{ov}+C_H+2W_2C_{ov}} = 0 \ldots. (25)$$

Because another approach to lowering the effect of charge injection incorporates both PMOS and NMOS devices such that the opposite charge packets injected by the two cancel each other. For Dq1 to cancel Dq2, we must have $W_1L_1C_{ox}$ (V_{CK} - V_{IN} - V_{THN}) = $W_2L_2C_{ox}$ (V_{IN} - V_{THP}).

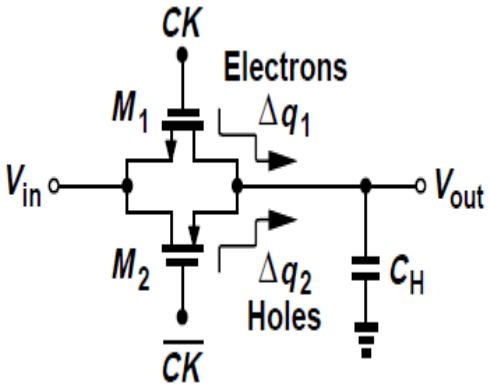


Fig 6: Use of complementary switches to reduce charge injection

V Conclusion:

In this work the charge sharing of switch capacitor and leakage power dissipation reduction through dummy switch capacitor with its source and drain terminal connected is propose. Process, operating voltage, and temperature variation were characterized to justify the benefit of BG-switches over conventional TG in a wide range of applications. With these design techniques building blocks necessary for switched-capacitor circuits can be implemented, enabling the creation of sampling, filtering, and data conversion circuits on low-voltage supplies. For simulation of switch capacitor circuit we will implement the switch capacitor circuits on 50nm CMOS technology on microwind 3.0 layout simulator tool

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